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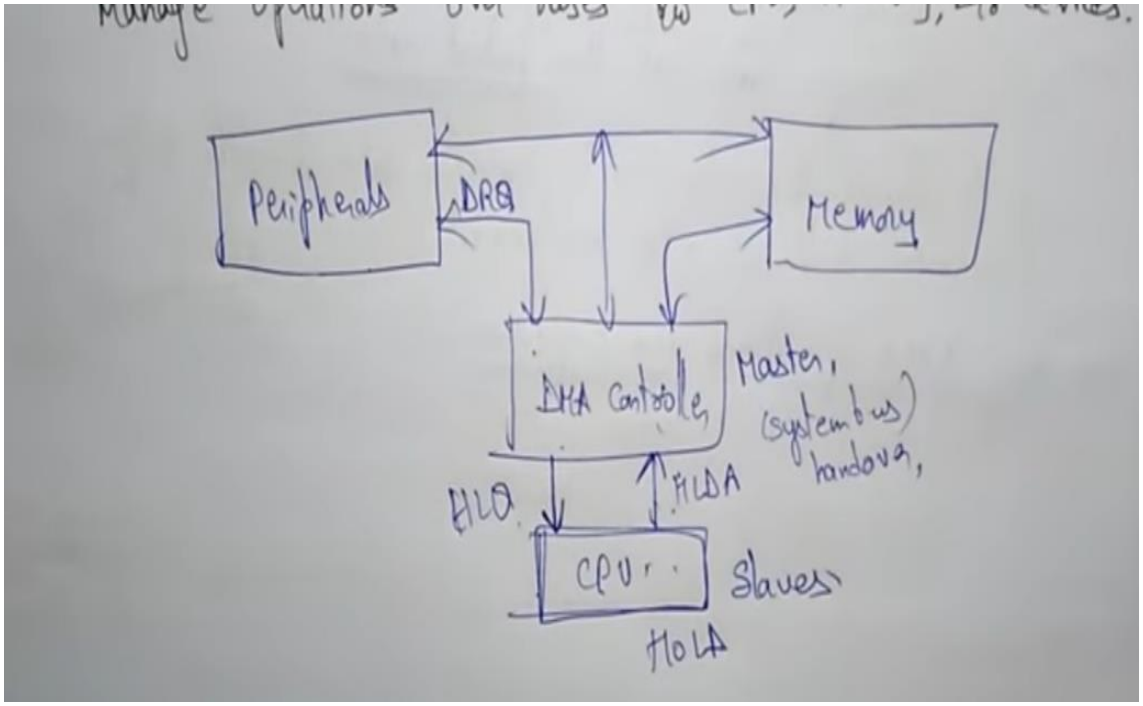
Bca 1st year

How DMA Operations are Performed?

Simply,



Following is the sequence of operations performed by a DMA –

Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.

The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.

Then the microprocessor all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request through HLDA signal.

Now the CPU is in

HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory, and I/O devices.

Features of 8257

Here is a list of some of the prominent features of 8257 −

It has four channels which can be used over four I/O devices.

Each channel has 16-bit address and 14-bit counter.

Each channel can transfer data up to 64kb.

Each channel can be programmed independently.

Each channel can perform read transfer, write transfer and verify transfer operations.

It generates MARK signal to the peripheral device that 128 bytes have been transferred.

It requires a single phase clock.

Its frequency ranges from 250Hz to 3MHz.

It operates in 2 modes, i.e., Master mode and Slave mode.